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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/809,761	03/14/2001	Martin Eugene Leonard	2001P04580US	4983

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Siemens Corporation
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EXAMINER	
YAO, KWANG BIN	
ART UNIT	PAPER NUMBER
2667	

DATE MAILED: 05/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/809,761	LEONARD, MARTIN EUGENE	
	Examiner	Art Unit	
	Kwang B. Yao	2667	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16,19 and 20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,19 and 20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 5-8, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Beckner et al. (US 4,642,630).

Beckner et al. discloses a communication system comprising the following features: regarding claim 1, a local area network, comprising: a) a data bus (Fig. 1, data bus 100) having a multiple of eight parallel data lines; b) a clock bus (Fig. 1, clock bus 53); c) a plurality of bus ports (Fig. 1, COMMUNICATIONS CONTROLLERS 3000-0, 3000-15) coupled to said data bus (Fig. 1, data bus 100) and said clock bus (Fig. 1, clock bus 53), each bus port (Fig. 1, COMMUNICATIONS CONTROLLER 3000-0) including a transceiver (Fig. 1, TRANSMITTER 3300, RECEIVER 3400) coupled to each of said data lines, an input buffer (Fig. 2, RCV DATA REG 3250) coupled to said transceiver (Fig. 1, TRANSMITTER 3300, RECEIVER 3400)s, an output buffer (Fig. 2, XMIT DATA REG 3240) coupled to said transceiver (Fig. 1, TRANSMITTER 3300, RECEIVER 3400)s, and a hardware interface (Fig. 1, FORMAT INTERFACE 3010; column 3, lines 9-11) coupled to said buffers, wherein at least two bus ports (Fig. 1, COMMUNICATIONS CONTROLLERS 3000-0, 3000-15) have different hardware interface (Fig. 1, FORMAT INTERFACE 3010; column 3, lines 9-11)s; regarding

claim 2, further comprising a power bus (Fig. 1, +V), each of said bus ports (Fig. 1, COMMUNICATIONS CONTROLLERS 3000-0, 3000-15) being coupled to said power bus (Fig. 1, +V) and drawing power therefrom; regarding claim 5, wherein data is transferred on the data bus (Fig. 1, data bus 100) in a repeating, variable length frame (Fig. 15, column 3, lines 43-45); regarding claim 6, wherein said frame is defined by a plurality of clock cycles (Fig. 1, CLOCK GEN 54), at least one of which is reserved for bidding for access to transmit on the data bus (Fig. 1, data bus 100); regarding claim 7, wherein each of said ports (Fig. 1, COMMUNICATIONS CONTROLLERS 3000-0, 3000-15) has a unique address (Fig. 2, ID REG 3210; column 11, lines 33-40) defining a unique priority value; regarding claim 8, wherein following the bidding cycle, access to the bus is granted to the port (Fig. 1, COMMUNICATIONS CONTROLLER 3000-0) having the highest priority and the other bidding port (Fig. 1, COMMUNICATIONS CONTROLLER 3000-0) addresses (Fig. 2, ID REG 3210; column 11, lines 33-40) are placed in a queue in order of priority; regarding claim 19, a) a data bus (Fig. 1, data bus 100) having a plurality of parallel data lines; and b) a clock bus (Fig. 1, clock bus 53) having a clock frequency; and c) a plurality of bus ports (Fig. 1, COMMUNICATIONS CONTROLLERS 3000-0, 3000-15) coupled to said data bus and said clock bus (Fig. 1, clock bus 53), wherein each of said bus ports has a configurable hardware interface (Fig. 1, FORMAT INTERFACE 3010; column 3, lines 9-11). See column 3-24.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 3, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beckner et al. (US 4,642,630) in view of Dunlap et al. (US 6,760,799).

Beckner et al. disclose the claimed limitations above. Beckner et al. does not disclose the following features: regarding claim 3, wherein said hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link; regarding claim 20, wherein said configurable hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link. Dunlap et al. discloses a system comprising the following features: regarding claim 3, wherein said hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link (column 2, lines 27-36); regarding claim 20, wherein said configurable hardware interfaces are selected from the group consisting of a serial port link, an Ethernet port link, a USB port link, and a FireWire (TM) port link (column 2, lines 27-36). It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Beckner et al., by using the features, as taught by Dunlap et al., in order to provide an efficient communication system by reducing the number of interrupts. See column 1, lines 5-7.

5. Claims 4, 9-16 rejected under 35 U.S.C. 103(a) as being unpatentable over Beckner et al. (US 4,642,630) in view of Osman et al. (US 6,760,799).

Beckner et al. disclose the claimed limitations above. Beckner et al. further discloses the following features: regarding claim 11, a parallel bus local area network, including a plurality of

ports (Fig. 1, COMMUNICATION CONTROLLER 3000-0, 3000-15) with each port (Fig. 1, COMMUNICATION CONTROLLER 3000-0) having a unique address (column 5, line 25 to column 6, line 7) assigned thereto defining a unique priority value, comprising: a) means for generating a repeating, variable length frame; b) port (Fig. 1, COMMUNICATION CONTROLLER 3000-0) control means for bidding for access to the bus during at least one predefined clock cycle of the frame; and c) a bus controller (Fig. 1, PROC 3001) for granting access to the bidding port (Fig. 1, COMMUNICATION CONTROLLER 3000-0) having the highest priority; regarding claim 15, d) means for enabling the port (Fig. 1, COMMUNICATION CONTROLLER 3000-0) having access to the data bus to transmit a message length during the message length cycle of the frame; and e) means for enabling (column 22, line 53 to column 23, line 68) the port (Fig. 1, COMMUNICATION CONTROLLER 3000-0) having access to the data bus to transmit a destination address during the destination address cycle of the frame. See column 1-24.

Beckner et al. does not disclose the following features: regarding claim 4, wherein said input and output buffers are each two kilobyte FIFOs; regarding claim 9, wherein each port maintains a copy of the queue; regarding claim 10, wherein following the bidding cycle, at least one cycle is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus; regarding claim 11, placing the other bidding port addresses in a queue; regarding claim 12, wherein each port maintains a copy of the queue; regarding claim 13, wherein bidding is only permitted when the queue is empty; regarding claim 14, wherein at least one cycle of the frame is reserved for transmission of

message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy signal on the data bus; regarding claim 16, f) means for enabling the port having the destination address to assert the busy signal during the busy cycle of the frame; and g) means for enabling the port attempting to transmit to the busy port to repeat bidding until the message is sent.

Osman et al. discloses a communication system comprising the following features; regarding claim 4, wherein said input and output buffers are each two kilobyte FIFOs (Fig. 4, INPUT FIFO 430, OUTPUT FIFO 460); regarding claim 9, wherein each port maintains a copy (column 10, lines 28-41) of the queue (Fig. 4, Address Lookup Logic 420, CAM 495); regarding claim 10, wherein following the bidding cycle, at least one cycle is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy (Fig. 8; column 13, line 38 to column 14, line 67) signal on the data bus; regarding claim 11, placing the other bidding port addresses in a queue (Fig. 4, Address Lookup Logic 420, CAM 495); regarding claim 12, wherein each port maintains a copy (column 10, lines 28-41) of the queue (Fig. 4, Address Lookup Logic 420, CAM 495); regarding claim 13, wherein bidding is only permitted when the queue (Fig. 4, Address Lookup Logic 420, CAM 495) is empty (Fig. 8, steps 845, 850); regarding claim 14, wherein at least one cycle of the frame is reserved for transmission of message length, at least one cycle is reserved for transmission of destination address, and at least one cycle is reserved for the port having the destination address to assert a busy (Fig. 8; column 13, line 38 to column 14, line 67) signal on the data bus; regarding claim 16, f) means for enabling the port having the destination address to assert the busy (Fig. 8; column 13, line 38 to

column 14, line 67) signal during the busy (Fig. 8; column 13, line 38 to column 14, line 67) cycle of the frame; and g) means for enabling the port attempting to transmit to the busy (Fig. 8; column 13, line 38 to column 14, line 67) port to repeat bidding until the message is sent. See column 6-17. It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the system Beckner et al., by using the features, as taught by Osman et al., in order to have an advantage to provide a high performance data transfer bus which includes buffer management that is simple and easy to implement the hardware. See Osman et al., column 3, lines 45-48.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Tang (US 6,296,067) discloses a distributed arbitration scheme.

Tang et al. (US 6,256,320) discloses a distributed arbitration scheme.

Kirtley Jr., et al. (US 4,608,700) discloses a digital data link.

Means et al. (US 4,373,183) discloses a data processing system.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kwang B. Yao whose telephone number is 571-272-3182. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chi H. Pham can be reached on 571-272-3179. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KWANG BIN YAO
PRIMARY EXAMINER

Kwang B. Yao
May 17, 2005